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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,840	11/25/2002	George M. Braceras	FIS920010332US1	9706
29154	7590	05/31/2005	EXAMINER	
FREDERICK W. GIBB, III MCGINN & GIBB, PLLC 2568-A RIVA ROAD SUITE 304 ANNAPOLIS, MD 21401			EJAZ, NAHEED	
			ART UNIT	PAPER NUMBER
			2631	

DATE MAILED: 05/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/065,840

Applicant(s)

BRACERAS ET AL.

Examiner

Ejaz Naheed

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on November 25, 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Specification***

1. The abstract of the disclosure is objected to because of the following:

Delete the title of the invention from the abstract. Correction is required. See MPEP § 608.01(b).

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C 102 that form the basis for the rejection under this section made in this office action:

A person shall be entitled to a patent unless —

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, 3, 4, 8, 9, 10, 14, 15, and 16 are rejected under 35 U.S.C 102(e) as being anticipated by Kirsch (US 6,812,799).

Refer to claim 1, Kirsch discloses a multiple clock signals having multiple rising edges (see figure 3), "a digital Delay-Lock-Loop (DLL) circuit comprising: a phase generator operable to produce a first clock signal having a first rising edge and a second clock signal having a second rising edge, wherein a timing difference between said first rising edge and said second rising edge is equal to a desired cycle time (see figure 3, col.6, lines 35-45); a delay circuit operable to receive said first clock signal and to produce a delayed clock signal (see figure 3, element 310, col.5, lines 59-67 and

col.6, lines 1-2); and a latch element connected to said delay circuit, said latch element operable to check whether said delayed clock signal is delayed by an amount equal to said desired cycle time (see figure 3, elements 320 and 310, col.6, lines 61-67 and col.7, lines 1-11).

Refer to claim 2, Kirsch discloses, 'a plurality of binary-weighted inverters, said inverters operable to adjust a delay of said delayed clock signals to be equal to said desired cycle time' (see figure 3, elements 302, col.6, lines 3-26).

As per claim 3, Kirsch inherently discloses 'phase-shift delay circuit connected to delay circuit, said phase-shifted delay circuit operable to produce a phase shift of said delayed clock signal'.

Regarding claim 4, Kirsch inherently discloses 'multiple degrees of phase shift'.

Refer to claim 8, Kirsch discloses a multiple clock signals (see figure 3) 'a digital Delay-Lock-Loop (DLL) circuit comprising: a phase generator receiving a clock signal and outputting a first clock line and a second clock line, wherein a timing difference between said first clock line and said second clock line is equal to a desired cycle time' (see figure 3, col.6, lines 35-45), 'a first delay circuit receiving said first clock line and outputting a delayed clock signal' (see figure 3, element 310, col.5, lines 59-67 and col.6, lines 1-2); 'a second delay circuit receiving said delayed clock signal and producing a phase shift of said delayed clock signal' (see figure 3, element 306, col.7, lines 57-67, col.8, lines 1-9), 'a latch element' (see figure 3, element 320), 'operatively connected to said first delay circuit (see figure 3, elements 310 and 320), 'wherein said latch element compares whether said delayed clock signal is delayed by an amount

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equal to said desired cycle time' (see figure 3, element 320, col.6, lines 61-67 and col.7, lines 1—11).

Refer to claim 9, Kirsch discloses, 'delay circuit comprises a plurality of serially connected binary-weighted delay elements' (see figure 3, elements 310, 316, and 322) and (column 2, lines 44-46), 'wherein said delay elements are operable to adjust a delay of said delayed clock signal to be equal to said desired cycle time' (see figure 3, col. 6, lines 30-60, col.7, lines 57-67, col.8, lines 1-12).

Refer to claim 10, Kirsch inherently discloses, 'phase shift comprises multiple degrees of phase shift'.

Refer to claim 14, Kirsch discloses a multiple clock signals having multiple rising edges (see figure 3), "a method of producing a phase shift in a digital Delay-Lock-Loop (DLL) circuit, said method comprising: generating a first clock signal having a first rising edge and a second clock signal having a second rising edge from a phase generator (see figure 3, col.6, lines 32-45) 'wherein a timing difference between said first rising edge and said second rising edge is equal to a desired cycle time(see figure 3, col.5, lines 59-64), 'sending said first clock signal to a delay circuit (see figure 3,col.5, lines 64-67), 'generating a delayed clock signal in said delay circuit (see figure 3, col.5, lines 64-67, col.6, lines 1-2), 'comparing a delay of said delayed clock signal with said desired cycle time in a latch element (see figure 3, element 320) and (col.6, lines 61-67, col.7, lines 1-11), 'wherein said delay circuit comprises said latch element (see figure 3, elements 320 and 322); and Kirsch inherently discloses 'generating a phase shift of said delayed clock signal in a phase-shifted delay circuit'.

Refer to claim 15, Kirsch discloses, 'the method of claim 14, further comprising adjusting said delay of said delayed clock signal to be equal to that of said desired cycle time' (see figure 3, elements 310, 316 and 322) and (col.6, lines 30-60, col.7, lines 57-67, col.8, lines 1-12), 'wherein said adjusting occurs in a plurality of binary-weighted inverters in said delay circuit' (see figure 3, elements 302, col.6, lines 3-26).

Refer to claim 16, Kirsch inherently discloses, 'wherein said phase shift comprises multiple degrees of phase shift'.

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 5, 6, 7, 17, 18, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kirsch (US 6,812,799) in view of Goto (775,696).

Refer to claim 5, Kirsch teaches all the limitations of the claim invention but he fails to show 'a filter connected to said latch element'.

Goto teaches, 'a filter (see figure 2), connected to said latch element, said filter operable to send a final value of said delayed clock signal to said phase-shifted delay circuit' (column 3, lines 51-55 and column 6, lines 20-24).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Goto into Kirsch as to convert input signal into control signal as taught by Goto (see column 4, lines 13-17).

As per claim 6, Kirsch teaches all the limitations of the claim invention but he fails to show 'a digital average function generator connected to said filter'.

Goto discloses, 'a digital average function generator (see figure 2, element 21) connected to said filter (see figure 2, element 22), wherein said digital average function generator is operable to instantaneously average previous comparisons of said delayed clock signal with said desired cycle time to produce said final value' (column 4, lines 5-13).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Goto into Kirsch as to represent an output signal which is a weighted average of input signals to a filter (see column 4, lines 9-13).

As per claim 7, Kirsch teaches all the limitations of the claim invention but he fails to show 'comparisons equal eight most recent previous comparisons'.

Goto discloses, 'wherein said previous comparisons equal eight most recent previous comparisons' (see figure 2, elements 13-16) and (column 4, lines 36-44).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Goto into Kirsch as to have phase comparators in order to generate an output signal in response to the phase difference as taught by Goto (see column 3, lines 55-63).

Refer to claim 17, Kirsch teaches all the limitations of the claim invention but he fails to disclose 'transferring is performed by filter connected to said latch element'.

Goto teaches 'transferring a final value of said delayed clock signal to said phase-shifted delay circuit, wherein said transferring is performed by a filter connected to said latch element' (see figure 2) and (column 4, lines 13-17 and column 6, lines 20-24).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Goto into Kirsch as to convert input signal into control signal as taught by Goto (see column 4, lines 13-17).

Refer to claim 18, Kirsch teaches all the limitations of the claim invention but he fails to disclose 'a digital average function generator connected to said filter'.

Goto discloses, 'The method of claim 17, further comprising averaging previous comparisons of said delayed clock signal with said desired cycle time to produce said final value, wherein said averaging occurs in a digital average function generator connected to said filter' (filter (see figure 2) and (column 4, lines 5-13).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Goto into Kirsch as to represent an output signal which is a weighted average of input signals to a filter as taught by Goto (see column 4, lines 9-13).

Refer to claim 19, Kirsch teaches all the limitations of the claim invention but he fails to show 'comparisons equal eight most recent previous comparisons'.

Goto discloses, 'wherein said previous comparisons equal eight most recent previous comparisons' (see figure 2, elements 13-16) and (column 4, lines 36-44).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Goto into Kirsch as to have phase comparators in order to generate an output signal in response to the phase difference as taught by Goto (see column 3, lines 55-63).

Refer to claim 20, Kirsch teaches all the limitations of the claim invention but he fails to show 'averaging occurs instantaneously'.

Goto teaches 'wherein said averaging occurs instantaneously' (see figure 2, element 21) and (column 4, lines 5-13).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Goto into Kirsch as to compare the average interstation delay time with delay time of the output signal in order to eliminate the effects of transmission line delay time on the system clock frequency as taught by Goto (see column 4, lines 54-59).

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kirsch (US 6,812, 799) in view of Stubbs et al. (US 2002/0057119), hereafter referred to as Stubbs.

Refer to claim 11, Kirsch teaches all the limitations of the claim invention but he fails to show a register connected to a latch element.

However, Stubbs discloses, 'a register' (see figure 2, element 208), 'register operable to send a final value of said delayed clock signal to said phase-shifted delay circuit (see figure 2, elements 208, 212, 216, and 218, page #3, paragraph # 0030 and 0031).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Stubbs into Kirsch as to indicate that each delay element of the delay line is operational as taught by Stubbs (see page # 2 and 3, paragraph # 0028).

7. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kirsch (US 6,812, 799) in view of Stubbs et al. (US 2002/0057119), hereafter referred to as Stubbs, and further in view of Goto (775,696)

As per claim 12, Kirsch and Stubbs teach all the limitations of the claim invention but they fail to show a digital average function generator.

Goto discloses 'digital average function generator is operable to instantaneously average previous comparisons of said delayed clock signal with said desired cycle time to produce said final value' (see figure 2) and (column 4, lines 5-12).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Goto into Kirsch and Stubbs as to represent an output signal which is a weighted average of input signals (see column 4, lines 9-13).

As per claim 13, Kirsch and Stubbs teach all the limitations of the claim invention but they fail to show 'comparisons equal eight most recent previous comparisons'.

Goto discloses phase comparators (see figure 2, elements 13-16) and (column 4, lines 36-44).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Goto into Kirsch and Stubbs as to have phase comparators in order to generate an output signal in response to the phase difference as taught by Goto (see column 3, lines 55-63).

***Conclusion***

8. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure. The Santou reference, US 6,879,321 filed on June 26, 2002 "Display Position Control Apparatus", The Noguti reference, U.S. 2002/0044325 published on 04/18/2002 "Out-of-Sync Detector, Receiver and Optical Receiver", The Baba et.al. reference, US 6,856,658 filed on 04/26/2000 "Digital PLL Circuit Operable in Short Burst Interval", The Yoon et al. reference, US 6,445,234 published on 09/03/2002 "Apparatus And Method For Accelerating Initial Lock Time Of Delayed Locked Loop", The Tomofuji et al. reference, US 2003/0039328 filed on 10/10/2002 "Timing Circuit", The Shrader et al. reference, US 6,665,230 filed on July 31, 2002 "Programmable Delay Compensation Circuit".

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naheed Ejaz whose telephone number is 571-272-5947. The examiner can normally be reached on Monday - Friday 8:00 - 4:30.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Naheed Ejaz  
Examiner  
Art Unit 2631

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**EMMANUEL BAYARD**  
**PRIMARY EXAMINER**